

cc

Notice of Allowability	Application No.	Applicant(s)	
	10/725,481	DRYNAN, JOHN M.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--


All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

- 1. ☒ This communication is responsive to 12/29/05.
 - 2. ☒ The allowed claim(s) is/are 47,49,50,52-59,61-71 and 73-78.
 - 3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 - 1. ☐ Certified copies of the priority documents have been received.
 - 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

- 4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 - 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
- 6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

- Attachment(s)**
- | | |
|---|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ | 7. <input type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____ |


 EUGENE LEE
 AW 2815

DETAILED ACTION.

Allowable Subject Matter

1. Claims 47, 49, 50, 52 thru 59, 61 thru 71, and 73 thru 78 allowed. The following is an examiner's statement of reasons for allowance: The references of record, either singularly or in combination, do not teach or suggest at least a memory device, comprising: a first conductive stud and a second conductive stud, said first and second conductive studs comprising epitaxial silicon; an interconnect line over and in electrical contact with said first conductive stud, an insulating sidewall separating said interconnect line from said second conductive stud, wherein said insulating sidewall extends to said second conductive epitaxial silicon stud through an insulating layer which is over and at least partially around said interconnect line.

Regarding claims 58, 59, and 61-63, the references of record, either singularly or in combination, do not teach or suggest at least at a DRAM cell structure, comprising: a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud; a bit line over and in electrical contact with said first conductive epitaxial stud; and an insulating sidewall structure separating said bit line from said second conductive epitaxial silicon stud, wherein said insulating sidewall structure is within a contact opening to said second conductive epitaxial silicon stud, wherein said contact opening extends through an insulating layer over and around said bit line.

Regarding claims 64-68, the references of record, either singularly or in combination, do not teach or suggest at least at a memory device, comprising: at least one first epitaxial silicon stud with a silicide cap and at least one second epitaxial silicon stud without a silicide cap; and a

Art Unit: 2815

conductive plug within said insulating sidewall and in electrical contact with said second epitaxial silicon stud.

Regarding claims 69-71, and 73-78, the references of record, either singularly or in combination, do not teach or suggest at least at a processor-based system, comprising: a first conductive epitaxial silicon stud and a second conductive epitaxial silicon stud; an interconnect line over and in electrical contact with said first conductive epitaxial stud; and an insulating sidewall structure separating said interconnect line from said second conductive epitaxial silicon stud, wherein said insulating sidewall structure extends to said second conductive epitaxial silicon stud through an insulating layer which is over and at least partially around said interconnect line.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee

January 22, 2006



AU 2815